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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,756	10/22/2003	Yow-Juang W. Liu	174/262	6692

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,756	LIU ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-14 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "*at least some of the transistors are included in the multiplexer*" in claim 11 and "*the additional transistors have higher threshold voltages than the plurality of transistors*" in claim 15 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 8-10, 12-14, 16, 18, 20 and 21are rejected under 35 U.S.C. 103(a) as being unpatentable over Sansbury (U. S. PAT. 5,959,891) in view of Rose et al (U. S. PAT. 5,471,421).

In claim 1, Sansbury teaches all claimed features in Figs. 2 and 4, a digital logic circuit comprising: a first region of logic (200); a second region of logic (adjacent 200); at least one pass transistor (410) that is coupled between the first and second regions of logic and that has a gate terminal, wherein the pass transistor prevents digital signals from the first region of logic from passing to the second region of logic when the pass transistor is off (open or non-conducting) and allows digital signals from the first region of logic to pass to the second region of logic when the pass transistor is on (closed or conducting); and control circuitry (400) coupled to the gate terminal of the pass transistor for selectively turning the pass transistor off and on, wherein the control circuitry turns the pass transistor on by applying a power supply voltage to the gate terminal; with the exception of teaching the control circuitry turns the pass transistor off by applying a reverse-bias voltage to the gate terminal. However, Rose et al. teaches in abstract a pass transistor receives a reverse bias voltage to switch the pass transistor into a substantially non-conducting state.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Sansbury and the teachings of Rose et al. in order to substantially reduce the leakage current through the pass transistor when it is on standby mode which results in saving power.

In claim 2, Sansbury further teaches the digital logic circuit defined in claim 1, wherein the control circuitry comprises a configuration random-access memory cell (col. 7, line 8).

In claim 3, Sansbury further teaches the digital logic circuit defined in claim 1, wherein the digital logic circuit is an integrated circuit (inherent), the digital logic circuit further comprising a plurality of transistors (410s) each of which is turned on and off by the control circuitry using the power supply voltage and the reverse-bias voltage (inherent).

In claim 4, Sansbury further teaches the digital logic circuit defined in claim 1, wherein the control circuitry comprises a configuration random-access memory cell (400) having an output coupled to the control gate of the transistor and having a programming data input to which programming data is provided (inherent), wherein the programming data determines whether the output coupled to the control gate turns the transistor on or off.

In claim 5, Sansbury further teaches the digital logic circuit defined in claim 1 further comprising: a first pin for receiving a power supply voltage (inherent); a second pin for receiving a ground voltage (inherent); and charge pump circuitry (col. 14, line 20)

that receives the power supply voltage and ground voltage and produces the reverse-bias voltage for the control circuitry (negative voltage).

In claim 8, Sansbury further teaches the digital logic circuit defined in claim 1, wherein the transistor (410) selectively connects two respective interconnection conductors (210 & 220) located between the first and second logic regions (200s).

Claims 9, 10, 12-14 correspond to detailed circuitry already discussed similarly with regard to claims 1-5 and 8.

In claim 16, Sansbury teaches all claimed features in Figs. 1, 2 and 4, a digital processing system comprising: a processor (101), a memory (105) coupled to the processor; and a digital logic circuit comprising: a first region of logic (200); a second region of logic (adjacent 200); at least one pass transistor (410) that is coupled between the first and second regions of logic and that has a gate terminal, wherein the pass transistor prevents digital signals from the first region of logic from passing to the second region of logic when the pass transistor is off (open or non-conducting) and allows digital signals from the first region of logic to pass to the second region of logic when the pass transistor is on (closed or conducting); and control circuitry (400) coupled to the gate terminal of the pass transistor for selectively turning the pass transistor off and on, wherein the control circuitry turns the pass transistor on by applying a power supply voltage to the gate terminal; with the exception of teaching the control circuitry turns the pass transistor off by applying a reverse-bias voltage to the gate terminal. However, Rose et al. teaches in abstract a pass transistor receives a reverse bias voltage to switch the pass transistor into a substantially non-conducting state.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Sansbury and the teachings of Rose et al. in order to substantially reduce the leakage current through the pass transistor when it is on standby mode which results in saving power.

In claim 18, Sansbury further teaches, the digital processing system defined in claim 16 further comprising input/output circuitry (111) coupled to the programmable logic device (121), the processor (101), and the memory (105).

In claim 20, Sansbury further teaches the digital processing system defined in claim 16, wherein the control circuitry (400) of the programmable logic device (121) comprises a memory cell that stores programming data (binary 0 or 1).

In claim 21, Sansbury further teaches the digial processing system in claim 16, wherein the digital logic circuit device further comprising: a first pin for receiving a power supply voltage (inherent); a second pin for receiving a ground voltage (inherent); and charge pump circuitry (col. 14, line 20) that receives the power supply voltage and ground voltage and produces the reverse-bias voltage for the control circuitry (negative voltage).

4. Claims 6, 7, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sansbury in view of Rose et al. as applied to claim 1 above, and further in view of Lee (U. S. PAT. 6,353,551).

In claim 6, Sansbury in view of Rose et al. teaches all claimed feature of claim 1; and Sansbury further teaches the digital circuitry comprises a programmable logic device (Fig. 2); the control circuitry (400) comprises a random-access memory cell

(SRAM) that is configuration selectively configured depending on which programming data is loaded (binary 0 or 1 is stored) into the configuration random-access memory cell. Lee teaches in Fig. 5 the configuration random-access memory has cross-coupled inverters (120) that store the programming data (the binary 0 or 1), wherein the programming data is received from a data line (Data in) that is selectively connected to the cross- coupled inverters in the random-access memory cell using an address line (ADDR).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the cross- coupled inverters in the random-access memory cell, as taught by Lee, with the teachings of Sansbury and Rose et al. to provide programmable logic device that is made using advanced integrated circuit fabrication techniques.

In claim 7, Rose et al. further teaches the digital logic circuit defined in claim 16 wherein the configuration random-access memory cell (20) further comprises at least one transistor (22) that is turned on with a power supply voltage (VDD) and is turned off using a reverse-bias voltage (VSS1).

In claim 17, Sansbury in view of Rose et al. teaches all claimed feature of claim 16; with the exception of teaching a circuit board on which the memory, the processor, and the programmable logic device are mounted. However, Lee teaches in Fig. 7, a circuit board (430) on which the memory (406), the processor (404), and the programmable logic device (402) are mounted.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine all the teachings in order to provide a digital processing system that can be used in a wide variety of applications, such as computer networking, data networking, video processing or any other application where the advantage of using reprogrammable logic is desirable.

In claim 19, Sansbury in view of Rose et al. teaches all claimed feature of claim 16; with the exception of teaching peripheral drivers coupled to the programmable logic device, the processor, and the memory. However, Lee teaches in Fig. 7, the digital processing system further comprising teaching peripheral drivers (410) coupled to the programmable logic device (402), the processor (404), and the memory (406).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine all the teachings in order to provide a digital processing system that can be used in a wide variety of applications, such as computer networking, data networking, video processing or any other application where the advantage of using reprogrammable logic is desirable.

5. No prior arts have been applied to claims 11 and 15.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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VIBOL TAN
PRIMARY EXAMINER